

APPLICATION MANUAL

RV-8564-C2

Real Time Clock / Calendar Module

DATE: February 2005

Revision No.: 1.2

Page 1/20

Headquarters: Micro Crystal
Div. of ETA SA
Mühlestrasse 14
CH-2540 Grenchen
Switzerland

Tel. +41 32 655 82 82
Fax +41 32 655 80 90
Internet www.microcrystal.ch
Email sales@microcrystal.ch

CONTENTS

1.0	Overview	3
1.1.	General Description	3
2.0	Block Diagram	3
2.1	Pinout	4
3.0	Functional Description	4
4.0	Absolute Maximum Ratings	5
4.1	Frequency Characteristics	5
4.2	DC Characteristics	5
5.0	Timing Characteristics I ² C bus	6
5.1	I ² C bus Timing Chart	6
6.0	Register Organization	7
6.1	Control and Status Register	7
6.2	Seconds, Minutes, Hours, Days	8
6.3	Weekdays	8
6.4	Months / Century	8
6.5	Years, Leap Year Compensation	8
6.6	Alarm Registers	9
6.7	CLKOUT Frequency Selection and Timer Register	9
6.8	CLKOUT-Frequency Output	9
6.9	Timer Control	9
7.0	Characteristics of the I ² C Bus	10
7.1	System Configuration	10
7.2	Start and Stop Condition	10
7.3	Bit Transfer	11
7.4	Acknowledge	11
7.5	Addressing	11
8.0	I ² C Bus Protocol	12
8.1	Write Mode	12
8.2	Read Mode at Specific Address	13
8.3	Read Mode	13
9.0	Package Dimensions and Solderpad Layout	14
9.1	Package Marking and Pin 1 Index	14
9.2	Recommended Reflow Temperature	15
9.3	Handling Precautions	16
10.0	Charts of Eletrical Characteristics	17
11.0	Packing Info Carrier Tape	18
11.1	Reel 13 Inch	19
12.0	Document Revision History	20



The I2C-BUS is a trademark of PHILIPS ELECTRONICS N.V.

RV-8564-C2

I²C-Bus Interface Real Time Clock / Calender Module

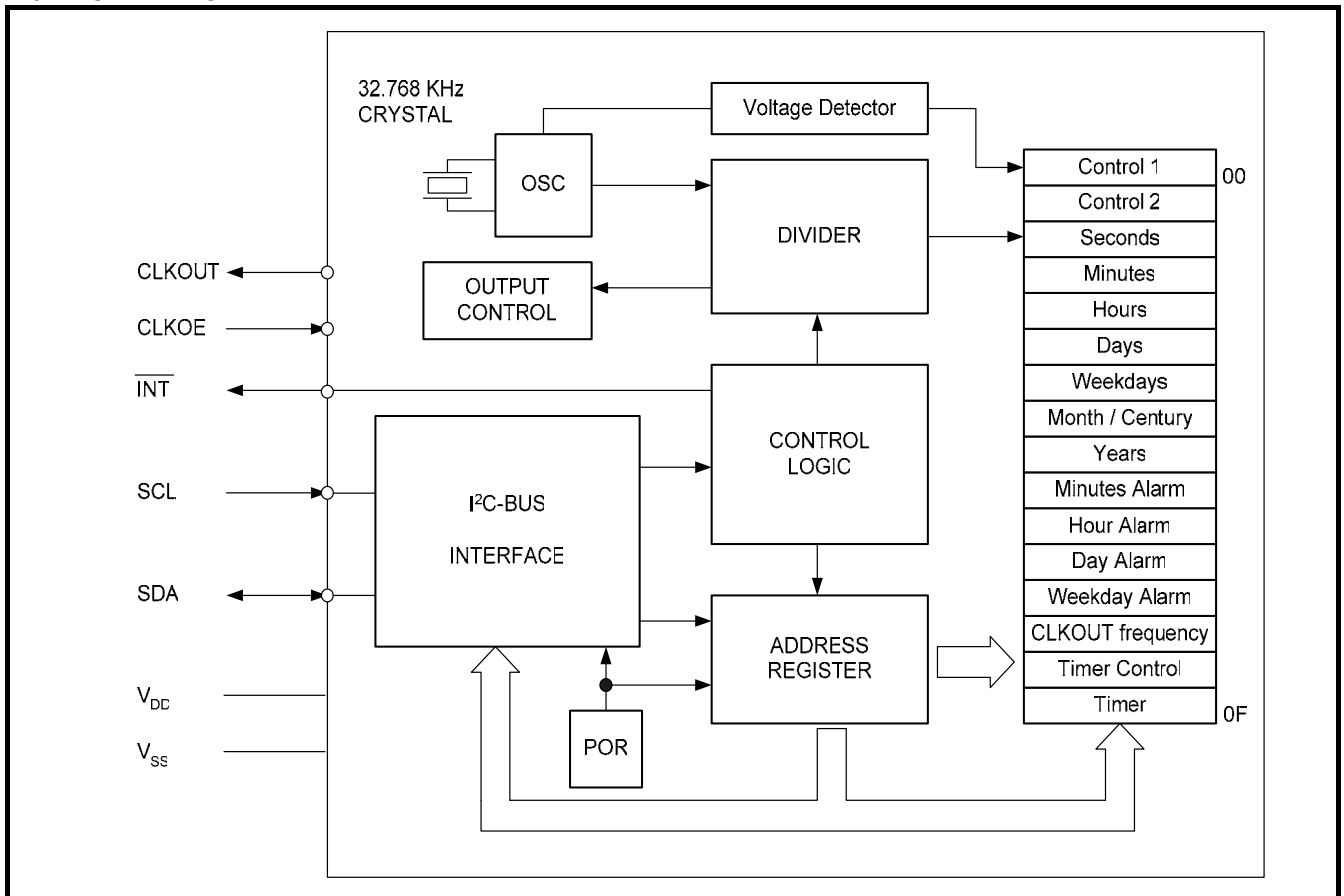
1.0 OVERVIEW

- RTC module with built-in crystal oscillating at 32'768kHz
- 100% lead-free product
- Small and compact package-size of 5.0 x 3.2 x 1.2mm
- 400kHz two-wire I²C Interface
- Wide Interface operating voltage: 1.8 – 5.5V
- Wide clock operating voltage: 1.2 – 5.5V
- Low power consumption: 250nA typ @ 3.0V / 25°C
- Provides year, month, day, weekday, hours, minutes, seconds
- Alarm and Timer functions
- Century flag
- Low-voltage detector, internal power-on reset
- Pogrammable clock output for peripheral devices (32.768kHz, 1024Hz, 32Hz, 1Hz)
- I²C slave address: read A3h, write A2h

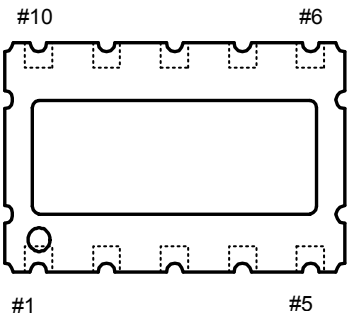
1.1 GENERAL DESCRIPTION

The RV-8564-C2 is a CMOS real-time clock/calendar optimized for low power consumption. A programmable clock output, interrupt output and voltage low detector are also provided. All address and data are transferred serially via a two-line bi-directional I²C bus. Maximum bus speed is 400kbit/sec. The built-in word address register is incremented automatically after each written or read data byte.

2.0 BLOCK DIAGRAM



2.1 PINOUT



# 1	V _{DD}	# 10	CLKOE
# 2	CLKOUT	# 9	N.C.
# 3	N.C	# 8	N.C.
# 4	SCL	# 7	INT
# 5	SDA	# 6	V _{SS}

3.0 FUNCTIONAL DESCRIPTION

The RV-8564-C2 RTC-module combines a RTC-IC with on-chip oscillator together with a 32.768kHz quartz crystal in a miniature ceramic-package. The RV-8564-C2 contains sixteen 8-bit registers with an auto-incrementing address register, a frequency divider which provides the source clock for the real time clock (RTC), a programmable clock output, a timer, a voltage-low detector and a 400kHz I²C bus interface.

All 16 registers are designed as addressable 8-bit parallel registers although not all bits are implemented.

The first two registers (memory address 00, 01) are used as control and/or status registers.

The memory addresses 02 through 08 are used as counters for the clock function (seconds up to year counters). Address locations 09 through 0C contain alarm registers which define the conditions for an alarm. Address 0D controls the CLKOUT output frequency. 0E and 0F are the timer control and timer registers, respectively.

The seconds, minutes, hours, days, weekdays, months, years as well as the minute alarm, hour alarm, day alarm and weekday alarm registers are all coded in BCD format.

When one of the RTC counters is read (memory locations 02 through 08), the contents of all counters are frozen at the beginning of a read cycle. Therefore, faulty reading of the clock/calendar during a carry condition is prevented.

ALARM FUNCTION MODES

By clearing the MSB of one or more of the alarm registers (AE = 'Alarm Enable'), the corresponding alarm condition(s) will be active. In this way an alarm can be generated from once per minute up to once per week. The alarm condition sets the alarm flag AF. The asserted AF can be used to generate an interrupt (INT). The AF may only be cleared by software.

TIMER

The 8-bit count-down timer at address 0F is controlled by the timer control register at address 0E. The timer control register determines one of 4 source clock frequencies for the timer (4096Hz, 64Hz, 1 sec, or 1 min), and enables/disables the timer. The timer counts down from a software-loaded 8-bit binary value. At the end of every countdown, the timer sets the timer flag TF. The TF may only be cleared by software. The asserted TF can be used to generate an interrupt (INT). The interrupt may be generated as a pulsed signal every countdown period or as a permanently active signal which follows the condition of the timer flag. TI/TP being used for this mode control. When reading the timer, the current countdown value is returned.

CLKOUT OUTPUT

A programmable square wave is available at the CLKOUT pin. Frequencies of 32768Hz, 1024Hz, 32Hz and 1Hz can be generated. CLKOUT is a CMOS push-pull output and if disabled it becomes logic zero.

RESET

The RV-8564-C2 includes an internal reset circuit which is active whenever the oscillator is stopped. In the reset state the I²C bus logic is initialized and all registers, including the address pointer, are cleared with the exception of bits FE, VL, TD1, TD0, TESTC and AE bits which are set to 1.

VOLTAGE LOW DETECTOR & CLOCK MONITOR

The RV-8564-C2 has an on-chip voltage low detector. When V_{DD} drops below V_{LOW} the 'Voltage Low' (VL, bit 7 in the seconds register) is set to indicate that the integrity of the clock information is no longer guaranteed. The VL flag can only be cleared by software. The VL bit is intended to detect the situation when V_{DD} is decreasing slowly for example under battery operation. Should V_{DD} reach V_{LOW} before power is re-asserted then the VL bit will be set. This will indicate that the time may be corrupted.

4.0 ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT
Supply voltage	V _{DD}	> GND / < V _{DD}	-0.5	+6.5	V
Supply current	I _{DD} ; I _{SS}	V _{DD} Pin	-50	+50	mA
Input voltage	V _I	Input Pin	GND -0.5	V _{DD} +0.5	V
Output voltage	V _O	INT Pin	GND -0.5	V _{DD} +0.5	V
DC Input current	I _I		-10	+10	mA
DC Output current	I _O		-10	+10	mA
Operating ambient temperature range	T _{OPR}		-40	+85	°C
Storage temperature range	T _{STO}	stored as bare product	-55	+125	°C

4.1 FREQUENCY CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	TYP.	MAX.	UNIT
Frequency precision	$\Delta F / F$	T _{AMB} = +25°C V _{DD} = 3.0 V		+/- 10 +/- 20	ppm
Frequency vs. voltage characteristics	$\Delta F / V$	T _{AMB} = +25°C V _{DD} = 1.8 V to 5.5 V	+/- 0.8	+/- 1.5	ppm / V
Frequency vs. temperature characteristics	$\Delta F / F_{OPR}$	T _{reference} = +25°C V _{DD} = 3.0 V		-0.035 ^{ppm} /°C (T _{OPR} -T _O) ² +/-10%	ppm
Turnover temperature	T _O		+25	+/-5	°C
Aging first year max.	V _O $\Delta F / F$	at 25°C		+/- 3	ppm
Oscillation start-up time	I _I		350	500	ms
CLKOUT duty cycle	T _{CLKOUT}	at 25°C	50	40 / 60	%

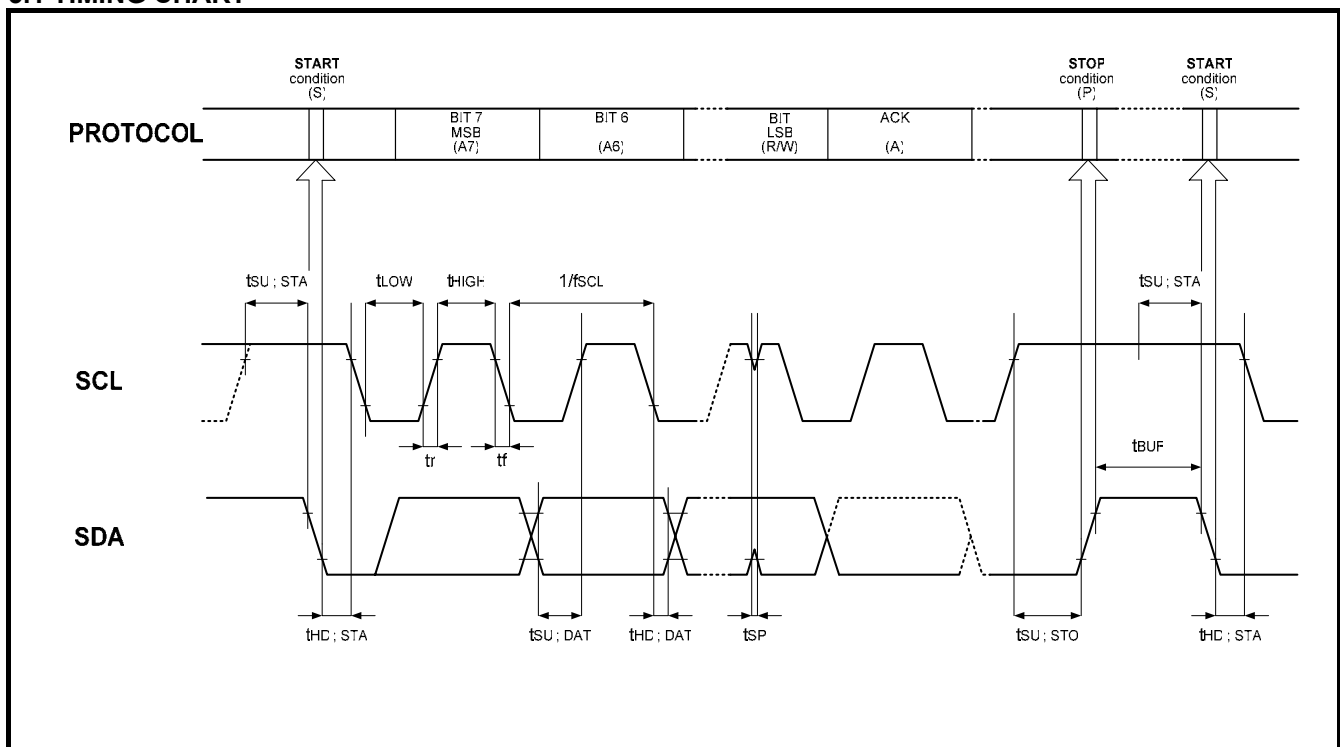
4.2 DC CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power Supply Voltage						
Supply voltage	V _{DD}	I ² C bus inactive, 25°C	1.0		5.5	V
		400kHz I ² C bus activity	1.8		5.5	V
Clock data integrity		25°C	V _{Low}		5.5	V
Power Supply Current						
Current consumption (I ² C bus activity)	I _{DDO}	f _{SCL} = 400kHz			800	μA
		f _{SCL} = 100kHz			200	μA
Current consumption (I ² C bus inactiv)	I _{DD}	f _{SCL} = 0 Hz, V _{DD} = 5.0V		275	550	nA
		f _{SCL} = 0 Hz, V _{DD} = 3.0V		250	500	nA
		f _{SCL} = 0 Hz, V _{DD} = 2.0V		225	450	nA
Current consumption CLKOUT = 32.768kHz, Load = 7.5pF	I _{DD32K}	f _{SCL} = 0 Hz, V _{DD} = 5.0V		2.5	3.4	μA
		f _{SCL} = 0 Hz, V _{DD} = 3.0V		1.5	2.2	μA
		f _{SCL} = 0 Hz, V _{DD} = 2.0V		1.1	1.6	μA
Inputs						
LOW level input voltage	V _{IL}		V _{SS} -0.5V		30% V _{DD}	V
HIGH level input voltage	V _{IH}		70% V _{DD}		V _{DD} +0.5V	V
Input leakage, INTN	I _{LI}	V _{DD} or V _{SS}			1	μA
Input capacitance	C _I				7	pF
Outputs						
SDA LOW output current	I _{OL(SDA)}	V _{OL} = 0.4V; V _{DD} = 5V			-3	mA
INT LOW output current	I _{OL(INT)}	V _{OL} = 0.4V; V _{DD} = 5V			-1	mA
CLKOUT LOW output current	I _{OL(CLKOUT)}	V _{OL} = 0.4V; V _{DD} = 5V			-1	mA
CLKOUT HIGH output current	I _{OH(CLKOUT)}	V _{OL} = 0.4V; V _{DD} = 5V			1	mA
Leakage current	I _{LO}	V _{DD} or V _{SS}	-1		1	μA
Voltage detector						
LOW voltage detection	V _{LOW}			0.9	1.1	V
Operating Temperature Range						
Operating temperature range	T _{OPR}		-40		+85	°C

5.0 TIMING CHARACTERISTICS I²C-BUS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
SCL clock frequency	fSCL			400	kHz
Start condition set-up time	tSU ; STA	0.6			µs
Start condition hold time	tHD ; STA	0.6			µs
Data set-up time	tSU ; DAT	100			ns
Data hold time	tHD ; DAT	0			ns
Stop condition set-up time	tSU ; STO	0.6			µs
Bus free time between STOP and START condition	tBUF	1.3			µs
SCL "LOW time"	tLOW	1.3			µs
SCL "HIGH time"	tHIGH	0.6			µs
SCL and SDA rise time	tr			0.3	µs
SCL and SDA fall time	tf			0.3	µs
Tolerance spike time on bus	tSP			50	ns

5.1 TIMING CHART



Note: The I²C-BUS access time between a START and a START condition or between a START and a STOP condition to this device must be less than one second.



The I2C-BUS is a trademark of PHILIPS ELECTRONICS N.V.

6.0 REGISTER ORGANIZATION

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	Control / Status 1	Test1	0	Stop	0	Test	0	0	0
01	Control / Status 2	0	X	0	TI / TP	AF	AF	AIE	TIE
02	Seconds	VL	40	20	10	8	4	2	1
03	Minutes	X	40	20	10	8	4	2	1
04	Hours	X	X	20	10	8	4	2	1
05	Days	X	X	20	10	8	4	2	1
06	Weekdays	X	X	X	X	X	4	2	1
07	Months / Century	C	X	X	10	8	4	2	1
08	Years	80	40	20	10	8	4	2	1
09	Minute Alarm	AD	40	20	10	8	4	2	1
0A	Hour Alarm	AD	X	20	10	8	4	2	1
0B	Day Alarm	AD	X	20	10	8	4	2	1
0C	Weekday Alarm	AD	X	X	X	X	4	2	1
0D	CLKOUT frequency	FE	X	X	X	X	X	FD1	FD0
0E	Timer Control	TE	X	X	X	X	X	TD1	TD0
0F	Timer	128	64	32	16	8	4	2	1

Bit positions labelled as "X" are not implemented.

6.1 CONTROL AND STATUS REGISTER

Control / Status 1

Stop: When set to 0 the RTC source clock runs. When set to 1, all RTC divider chain flip flops are asynchronously set to 0; the RTC clock is stopped. (CLKOUT at 32.768kHz is still available)

Test: The two bits, TEST and TEST1, are for device testing. Make sure TEST bits are set to 0 during normal operation. If accidentally set to 1, they may modify the clock-data or result in abnormal time.

Control / Status 2

AF, TF: Alarm Flag, Timer Flag

When an alarm occurs, AF is set to 1. Similarly, at the end of a timer countdown, TF is set to 1. These bits maintain their value until overwritten by software. If both timer and alarm interrupts are required in the application, the source of the interrupt can be determined by reading these bits. To prevent one flag being overwritten while clearing another, a logic AND is performed during a write access.

Write '1' to AF or TF: No change to flag
Write '0' to AF or TF: Respective flag is cleared.

TI/TP: Timer Interrupt/ Timer Periodic INT mode.
TI/TP = 0: INT is active when TF is active. (subject to the status of TIE).

AIE, TIE: Alarm Interrupt Enable, Timer Interrupt

Enable These bits activate or deactivate the generation of an interrupt when AF or TF is asserted, respectively. The interrupt is the logical OR of these two conditions when both AIE and TIE are set.

TI/TP: Timer Interrupt/ Timer Periodic $\overline{\text{INT}}$ mode.
TI/TP = 0: $\overline{\text{INT}}$ is active when TF is active. (subject to the status of TIE).
TI/TP = 1: $\overline{\text{INT}}$ pulses active according to the below table. (subject to the status of TIE).

$\overline{\text{INT}}$ Operation (TI/TP=1)

Timer Source Clock	$\overline{\text{INT}}$ Period	
	n>1	n=1
4096 Hz	1/4096 seconds	1/8192 seconds
64Hz	1/64 seconds	1/128 seconds
1Hz	1/64 seconds	1/64 seconds
1/60Hz	1/64 seconds	1/64 seconds

6.2 SECONDS, MINUTES, HOURS, DAYS

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
02	Seconds	VL	40	20	10	8	4	2	1
03	Minutes	X	40	20	10	8	4	2	1
04	Hours	X	X	20	10	8	4	2	1
05	Days	X	X	20	10	8	4	2	1

These registers contain the respective time and date values coded in BCD format.

Example: seconds register contains 'x1011001' = 59 seconds. The RV-8564-C2 stores the time of day in 24-hour format.

Note: Bit 7 of the seconds register is used to return the 'Voltage Low' (VL) detection bit.

6.3 WEEKDAYS

Address	Day	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
06	Sunday	X	X	X	X	X	0	0	0
06	Monday	X	X	X	X	X	0	0	1
06	Tuesday	X	X	X	X	X	0	1	0
06	Wednesday	X	X	X	X	X	0	1	1
06	Thursday	X	X	X	X	X	1	0	0
06	Friday	X	X	X	X	X	1	0	1
06	Saturday	X	X	X	X	X	1	1	0

The weekday register has a bit assignment as shown in the table above. Only the 3 LSBs are utilized.

6.4 MONTHS / CENTURY

Address	Month	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
07	January	C	X	X	0	0	0	0	1
07	February	C	X	X	0	0	0	1	0
07	March	C	X	X	0	0	0	1	1
07	April	C	X	X	0	0	1	0	0
07	May	C	X	X	0	0	1	0	1
07	June	C	X	X	0	0	1	1	0
07	July	C	X	X	0	0	1	1	1
07	August	C	X	X	0	1	0	0	0
07	September	C	X	X	0	1	0	0	1
07	October	C	X	X	1	0	0	0	0
07	November	C	X	X	1	0	0	0	1
07	December	C	X	X	1	0	0	1	0

The months/century register utilizes the 5 LSBs to encode the month of the year as shown in the table below.

Bit 7 of the months/century register also contains the century indicator.

When C=0, the century is 20xx, when C=1 the century is 19xx. This bit is toggled when the years register overflows from 99 to 00.

6.5 YEARS, LEAP YEAR COMPENSATION

Address	Years	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
08	Years	80	40	20	10	8	4	2	1

The years register encodes the two lower year digits in BCD format according to the table above.

When the years register overflows from 99 to 00, the century bit C in the months/century register is toggled.

Leap Year Compensation.

The RV-8564-C2 compensates for leap years by adding a 29th day to February if the year counter contains a value which is divisible by 4, including the year 00.

6.6 ALARM REGISTERS

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
09	Minute Alarm	AD	40	20	10	8	4	2	1
0A	Hour Alarm	AD	X	20	10	8	4	2	1
0B	Day Alarm	AD	X	20	10	8	4	2	1
0C	Weekday Alarm	AD	X	X	X	X	4	2	1

AD = 0: Alarm enable: Compare Alarm register with current time.

AD = 1: Ignore Alarm register

The registers at addresses 09h through 0Ch contain alarm information.

When one or more of these registers is loaded with a valid minute, hour, day or weekday and its corresponding 'Alarm Disable' (AD, bit 7) is '0', then that information will be compared with the current minute, hour, day and weekday.

When all enabled comparisons first match, the 'Alarm Flag' (AF, bit 3 in control/status 2 register) is set.

AF will remain set until cleared by software. Once AF has been cleared it will only be set again when the time increments to match the alarm condition once more.

Alarm registers which have their 'Alarm Disable' bit at '1' will be ignored, combining the AD-bits 7; a highly versatile alarm can be set.

When all AD-bits 7 are set to '1', no alarm will occur.

6.7 CLKOUT FREQUENCY SELECTION AND TIMER REGISTER

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0D	CLKOUT Frequency	FE	X	X	X	X	X	FD1	FD0
0E	Timer Control	TE	X	X	x	x	x	TD1	TD0
0F	Timer	128	64	32	16	8	4	2	1

6.8 CLKOUT /FREQUENCY-OUTPUT

Output Frequency	FD1	FD0
32768 Hz	0	0
1024 Hz	0	1
32 Hz	1	0
1 Hz	1	1

The CLKOUT pin is controlled by two signals; the Frequency enable (FE bit 7) and CLKOUT output-enable pin 10 (CLKOE).

FE and CLKOE

FE	CLKOE	CLKOUT
0	0	0
0	1	0
1	0	0
1	1	Selected Frequency

6.9 TIMER CONTROL

The timer register is an 8-bit binary countdown timer. It is enabled/disabled via the timer control register, Timer Enable (TE, bit 7)

TE = 0: Timer is disabled.

TE = 1: Timer is enabled (i.e timer counts down)

Timer Source Clock	TD1	TD0
4096 Hz	0	0
64 Hz	0	1
1 Second	1	0
1 Minute	1	1

TD1, TD0: Timer source clock frequency select.

These bits determine the source clock for the countdown timer (address 0Fh).

When not in use, TD1 & TD0 should be set to 1/60Hz for power saving.

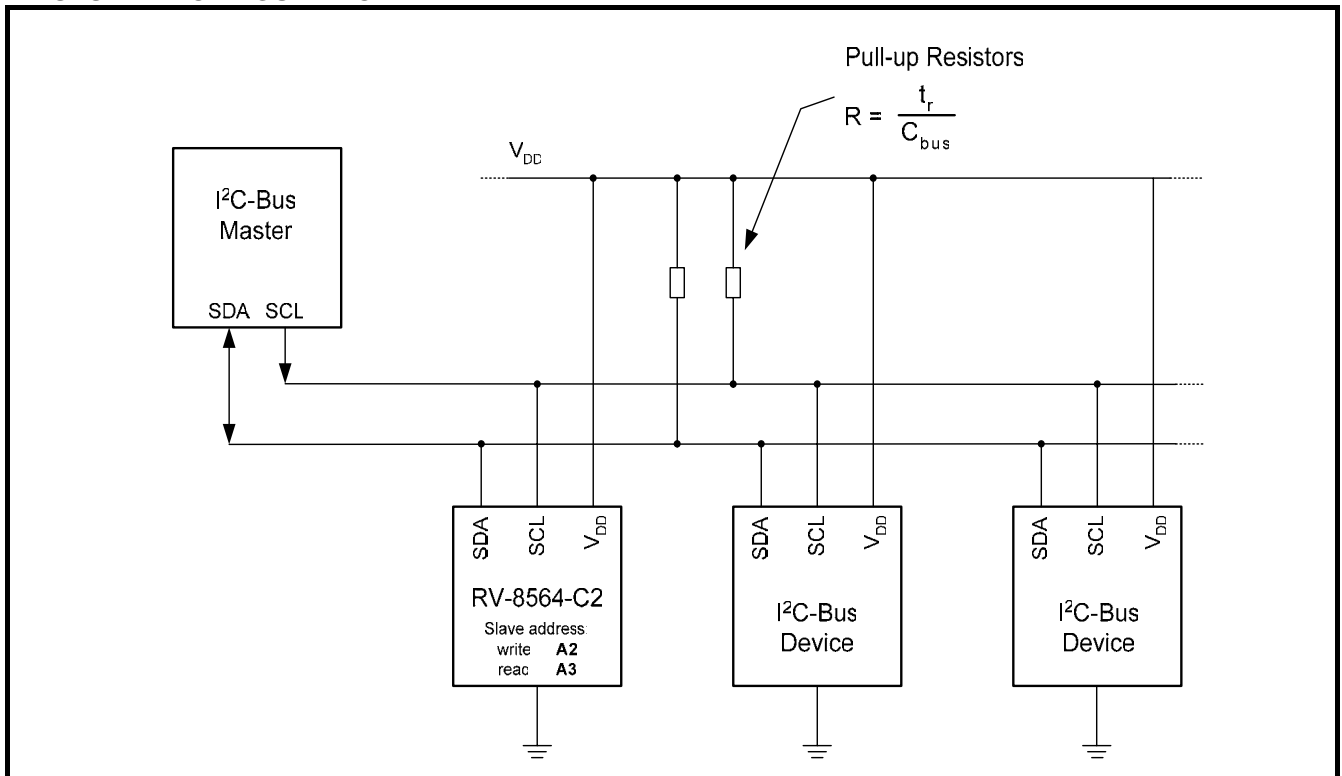
The source clock for the timer is also selected by the timer control register. Other timer properties such as single or periodic interrupt generation are controlled via the control/status 2 register (address 01h).

For accurate read back of the count down value, the I²C clock (SDA) must be operating at a frequency of at least twice the selected timer clock.

7.0 CHARACTERISTICS OF THE I²C BUS

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial-Dataline (SDA) and a Serial-Clockline (SCL). SCL and SDA ports are open-drain or open-collector architecture to allow connections of multiple devices. Both lines must be connected to a positive supply via pull-up resistors. Data transfer may be initiated only when the bus is not busy.

7.1 SYSTEM CONFIGURATION



Since multiple devices can be connected with the I²C-bus, all I²C-bus devices have a fixed, unique device number built-in to allow individual addressing of each device.

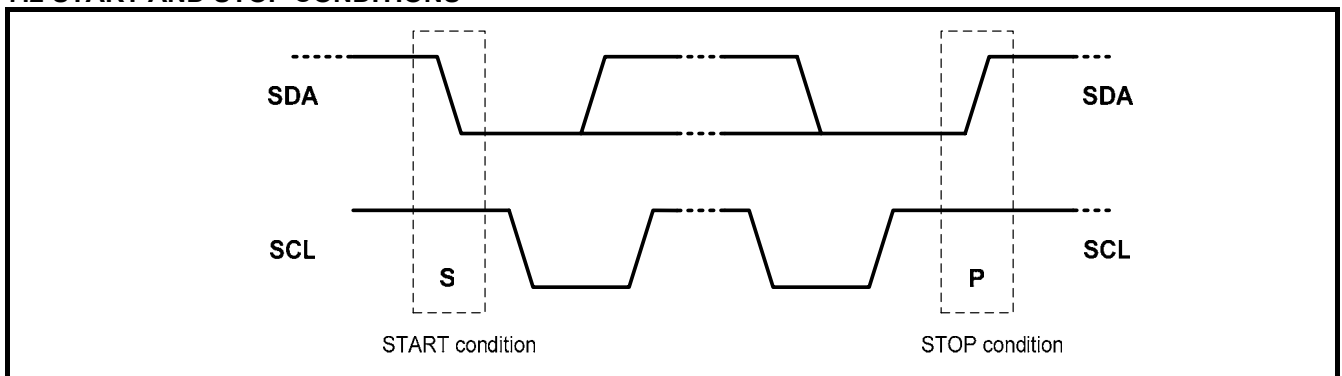
The device that controls the I²C-bus is the “Master”, the devices which are controlled by the master are the “Slaves”. A device generating a message is a “Transmitter”, a device receiving a message is the “Receiver”. The RV-8564-C2 acts as a Slave-Receiver or Slave-Transmitter.

Before any data is transmitted on the I²C -bus, the device which should respond is addressed first.

The addressing is always carried out with the first byte transmitted after the start procedure.

Therefore the clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line.

7.2 START AND STOP CONDITIONS

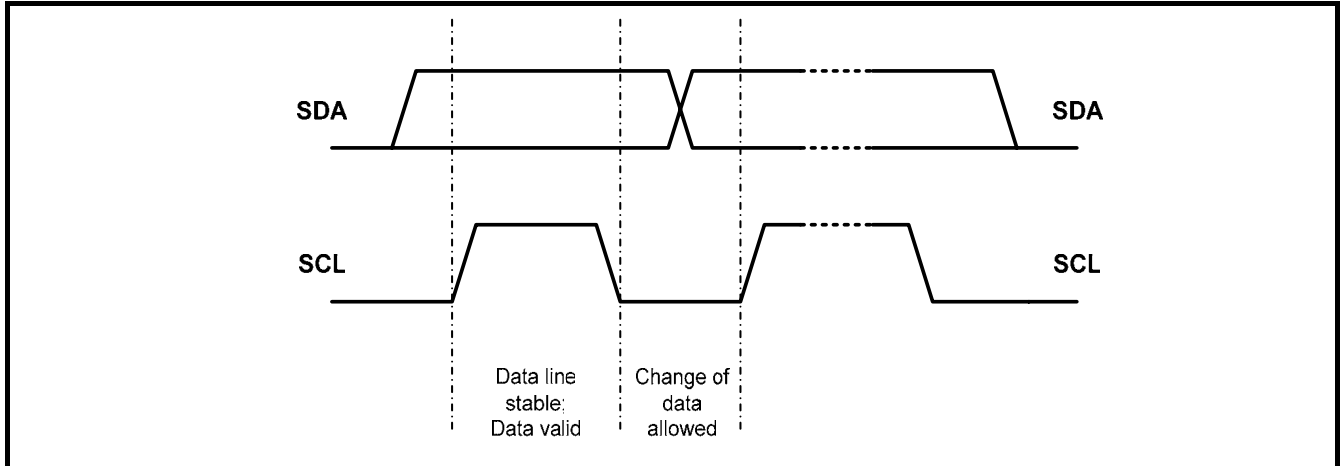


Both, SDA data and SCL clock-lines remain HIGH when the bus is not busy.

A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the start condition (S).

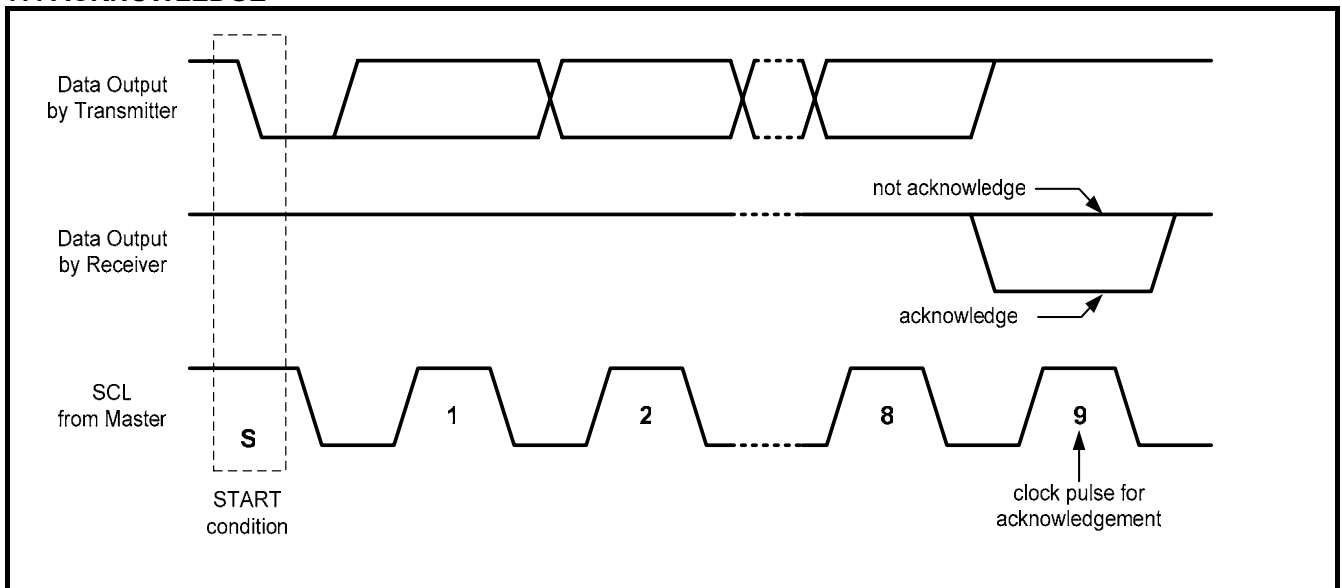
A LOW-to-HIGH transition of the data line, while the clock is HIGH, is defined as the stop condition (P).

7.3 BIT TRANSFER



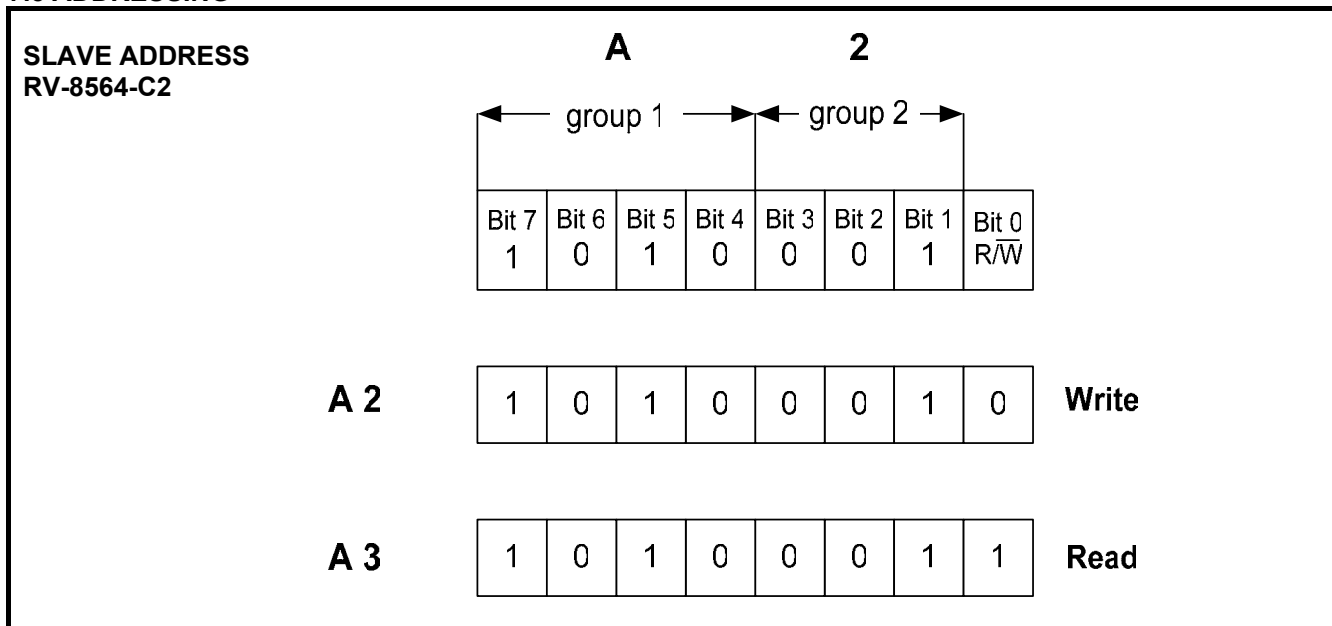
1 Data Bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse, data change should be executed during the LOW period of the clock pulse.

7.4 ACKNOWLEDGE



There is no limit to the numbers of data bytes transmitted between the start and stop conditions. Each byte (of 8 bits) is followed by an acknowledge bit. Therefore, the Master generates an extra acknowledge-clock pulse. The acknowledge bit is a HIGH level signal put on the SDA line by the Transmitter-Device, the Receiver-Device must pull down the SDA line during the acknowledge-clock-pulse to confirm the correct reception of the last byte. Either a Master-Receiver or a Slave-Receiver which is addressed must generate an acknowledge after the correct reception of each byte. The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. (set-up and hold times must be taken into consideration). If the Master is addressed as Receiver, it can stop data transmission by **not** generating an acknowledge on the last byte that has been sent from the Slave Transmitter. In this event, the Slave-Transmitter must leave the data line HIGH to enable the Master to generate a stop condition.

7.5 ADDRESSING

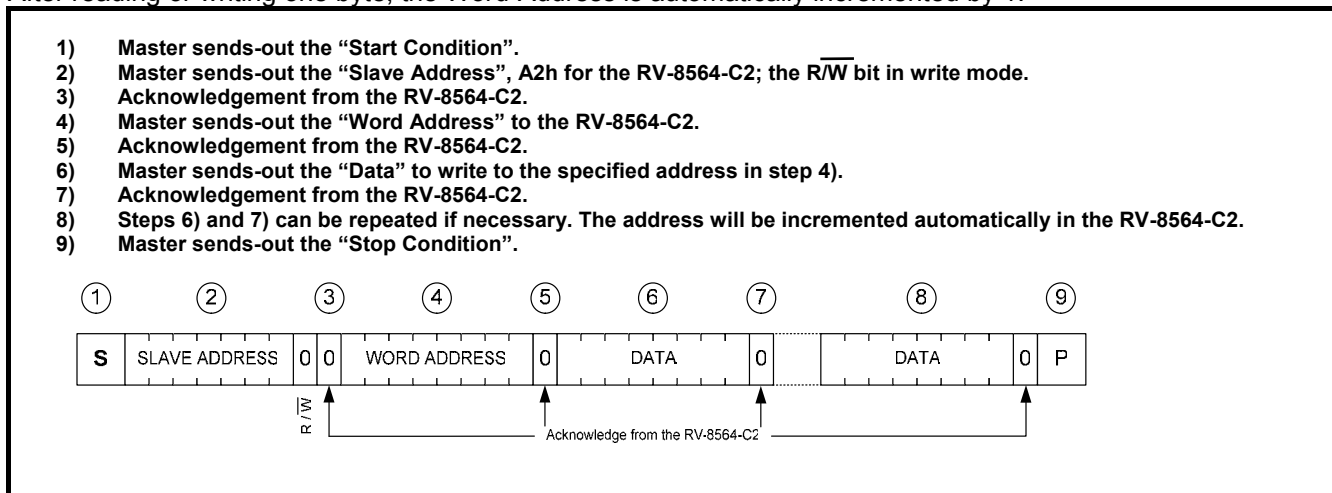


8.0 I²C BUS PROTOCOL

Before any data is transmitted on the I2C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure. The RV-8564-C2 acts as a slave receiver or slave transmitter. Therefore the clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line.

8.1 WRITE MODE

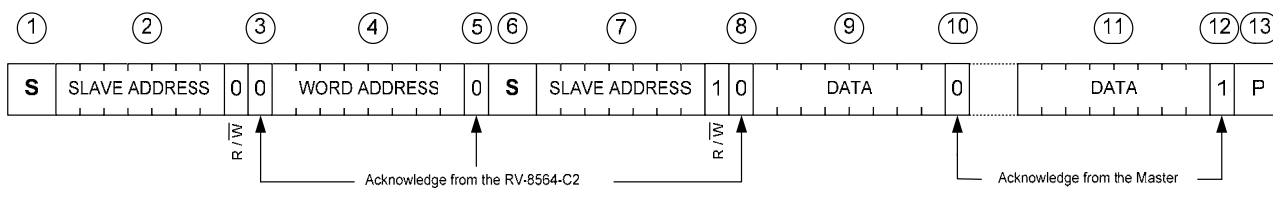
Master transmits to Slave-Receiver at specified address
 The Word-Address is four bit value that defines which register is to be accessed next.
 The upper four bits of the Word-Address are not used.
 After reading or writing one byte, the Word-Address is automatically incremented by 1.



8.2 READ MODE AT SPECIFIC ADDRESS

Master reads Data after setting Word Address

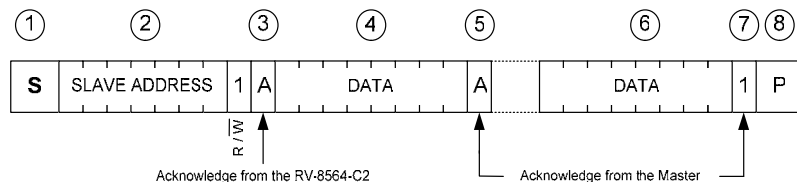
- 1) Master sends-out the "Start Condition".
- 2) Master sends-out the "Slave Address", A2h for the RV-8564-C2; the $\overline{R/W}$ bit in write mode.
- 3) Acknowledgement from the RV-8564-C2.
- 4) Master sends-out the "Word Address" to the RV-8564-C2.
- 5) Acknowledgement from the RV-8564-C2.
- 6) Master sends-out the "Start Condition". "Stop Condition" has not been sent.
- 7) Master sends-out the "Slave Address", A3h for the RV-8564-C2; the $\overline{R/W}$ bit in read mode.
- 8) Acknowledgement from the RV-8564-C2.
At this point, the Master becomes a Receiver, the Slave becomes the Transmitter.
- 9) The Slave sends-out the "Data" from the Word Address specified in step 4).
- 10) Acknowledgement from the Master.
- 11) Steps 9) and 10) can be repeated if necessary. The address will be incremented automatically in the RV-8564-C2.
- 12) The Master, addressed as Receiver, can stop data transmission by not generating an acknowledge on the last byte that has been sent from the Slave Transmitter. In this event, the Slave-Transmitter must leave the data line HIGH to enable the Master to generate a stop condition.
- 13) Master sends-out the "Stop Condition".



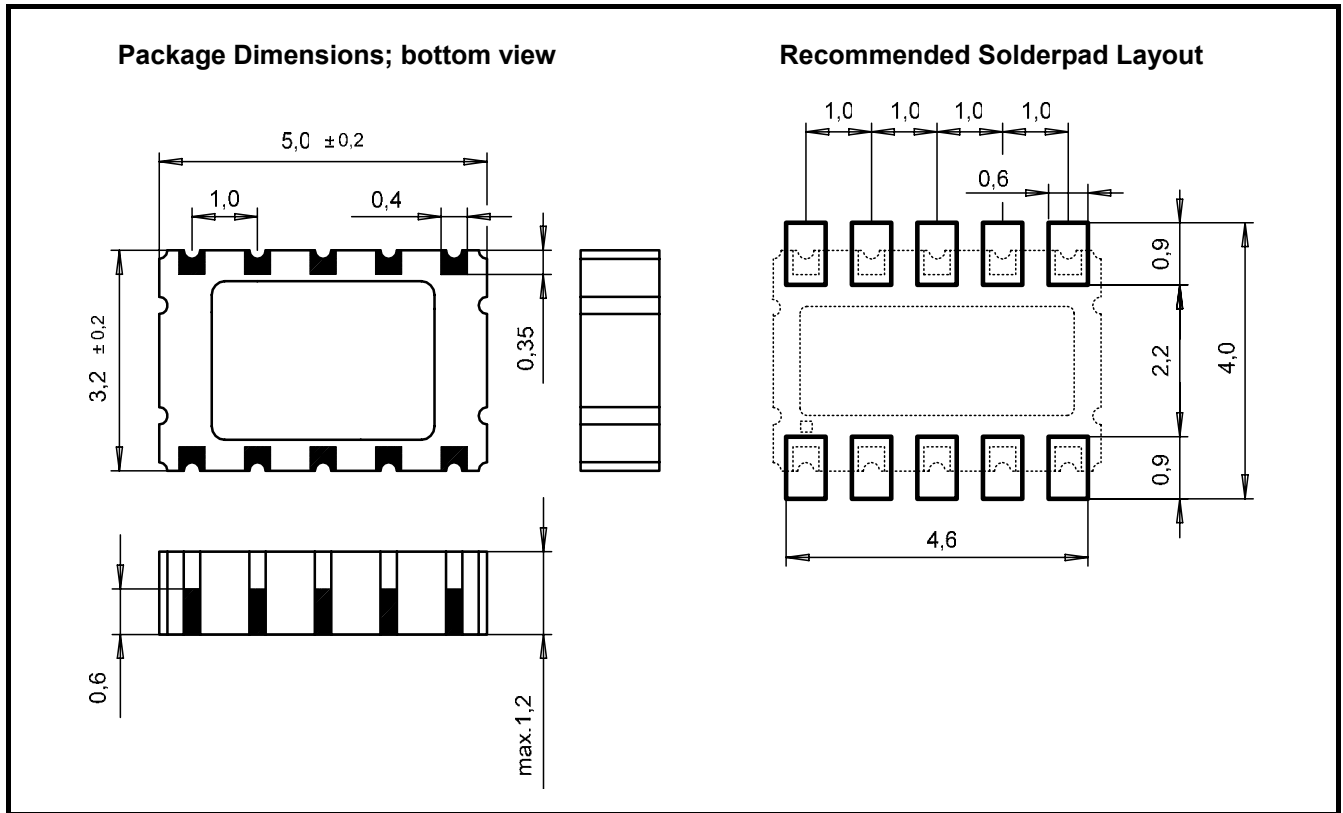
8.3 READ MODE

Master reads Slave-Transmitter immediately after first byte

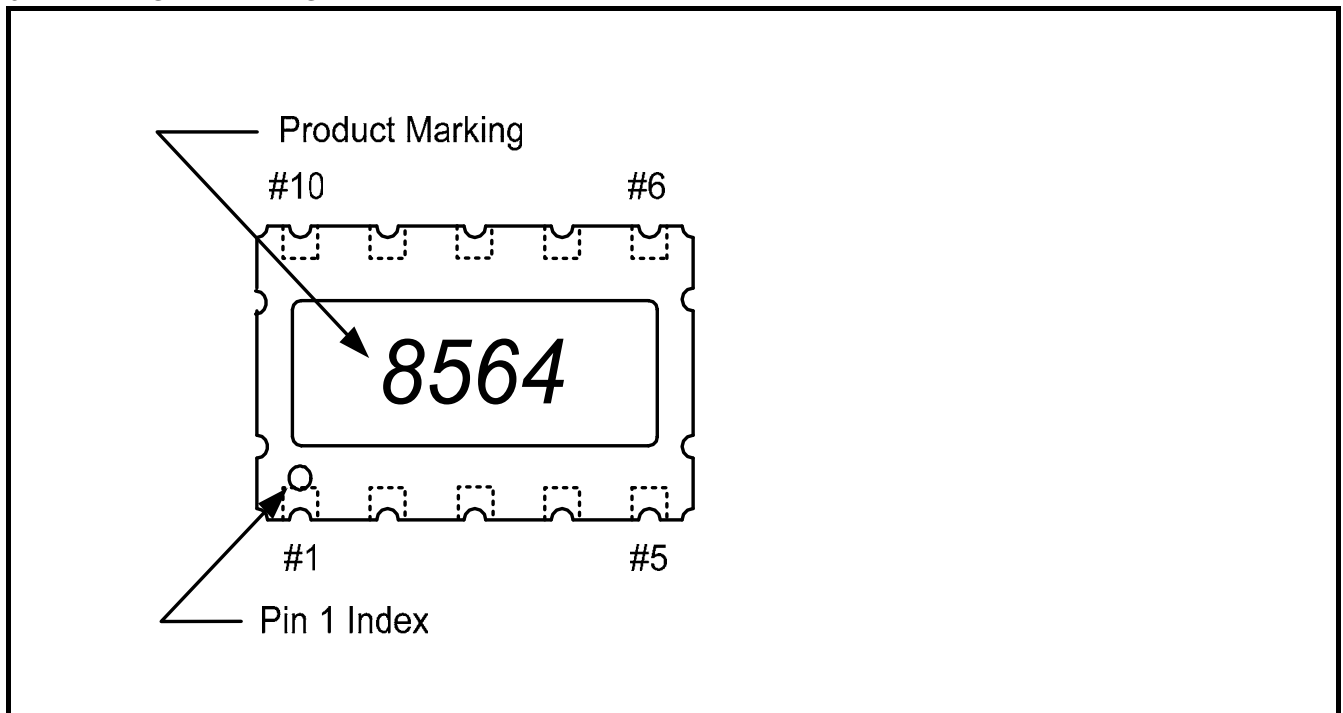
- 1) Master sends-out the "Start Condition".
- 2) Master sends-out the "Slave Address", A3h for the RV-8564-C2; the $\overline{R/W}$ bit in read mode.
- 3) Acknowledgement from the RV-8564-C2.
At this point, the Master becomes a Receiver, the Slave becomes the Transmitter
- 4) The RV-8564-C2 sends-out the "Data" from the last accessed Word Address incremented by 1.
- 5) Acknowledgement from the Master.
- 6) Steps 4) and 5) can be repeated if necessary. The address will be incremented automatically in the RV-8564-C2.
- 7) The Master, addressed as Receiver, can stop data transmission by not generating an acknowledge on the last byte that has been sent from the Slave Transmitter. In this event, the Slave-Transmitter must leave the data line HIGH to enable the Master to generate a stop condition..
- 8) Master sends-out the "Stop Condition".



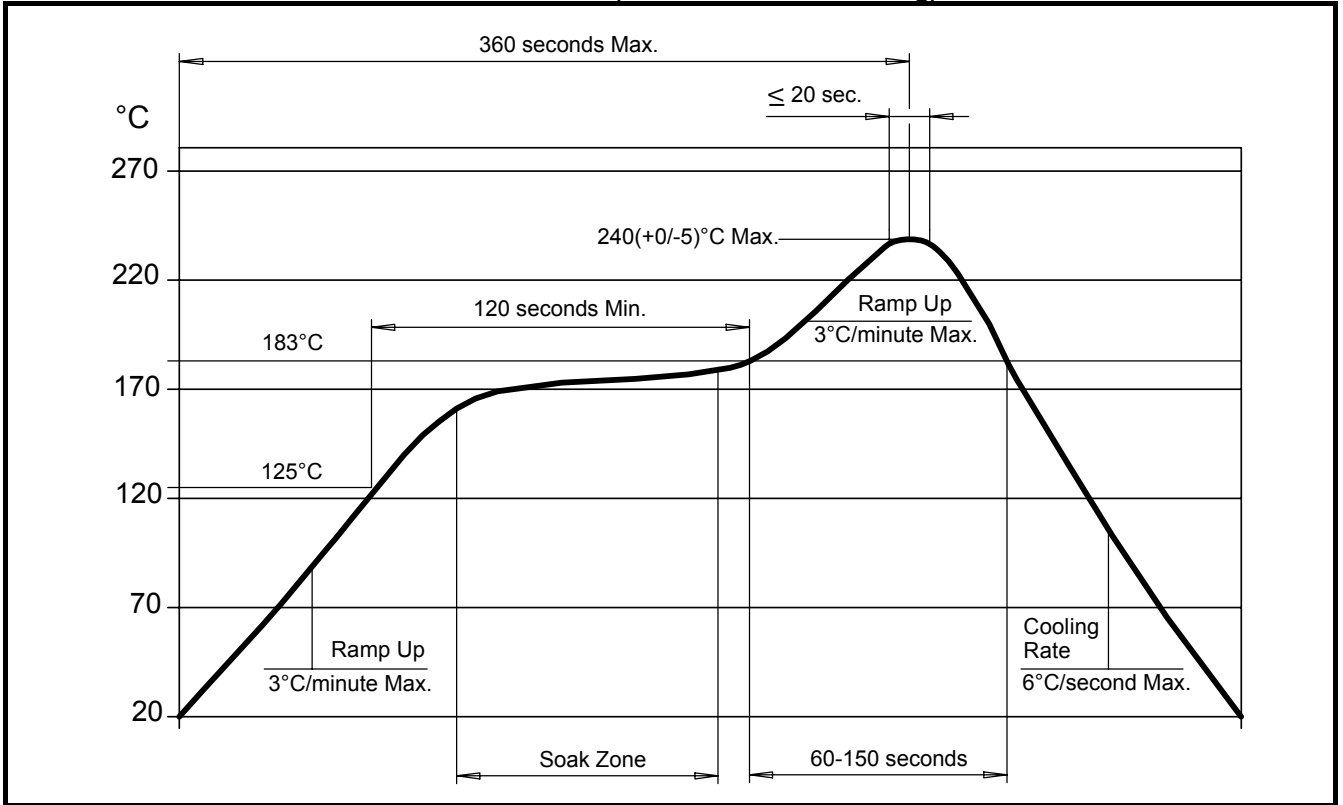
9.0 PACKAGE DIMENSIONS AND SOLDERPAD LAYOUT



9.1 PACKAGE MARKING AND PIN 1 INDEX



9.2 RECOMMENDED REFLOW TEMPERATURE (for "lead-free" soldering)



9.2 HANDLING PRECAUTIONS FOR CRYSTALS

The built-in tuning-fork crystal consists of pure Silicon Dioxide in crystalline form. The cavity inside the package is evacuated and hermetically sealed in order for the crystal blank to function undisturbed from air molecules, humidity and other influences.

Shock and vibration

Keep the crystal from being exposed to **excessive mechanical shock and vibration**. Micro Crystal guarantees that the crystal will bear a mechanical shock of 5000g / 0.3 ms.

The following special situations may generate either shock or vibration:

Multiple PCB panels - Usually at the end of the pick & place process the single PCBs are cut out with a router. These machines sometimes generate vibrations on the PCB that have a fundamental or harmonic frequency close to 32.768 kHz. This might cause breakage of crystal blanks due to resonance. Router speed should be adjusted to avoid resonant vibration.

Ultrasonic Cleaning - Avoid cleaning processes using ultrasonic energy. These processes can damage crystals due to mechanical resonance of the crystal blank.

Overheating, Rework high-temperature-exposure

Avoid overheating the package. The package is sealed with a sealring consisting of 80% Gold and 20% Tin. The eutectic of this alloy is at 280°C. Heating the sealring up to >280°C will cause melting of the metal seal which then, due to the vacuum, is sucked into the cavity forming an air duct. This happens when using hot-air-gun set at temperatures >300°C.

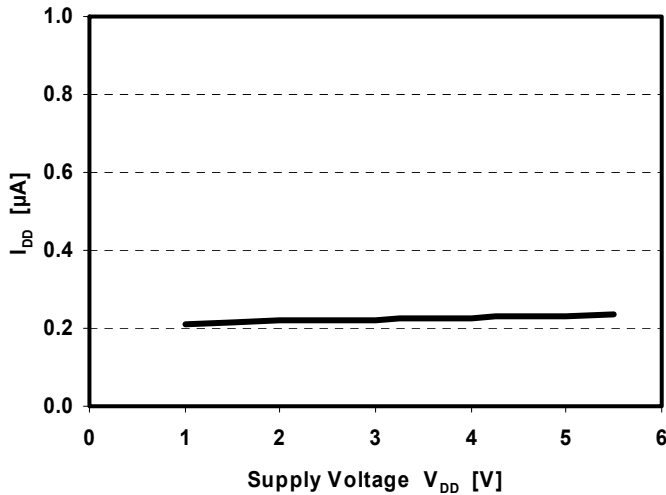
Use the following methods for re-work:

- Use a hot-air- gun set at 260°C
- Use 2 temperature-controlled soldering irons, set at 260°C, with special-tips to contact all solder-joints from both sides of the package at the same time, remove part with tweezers when pad solder is liquid.

10.0 CHARTS OF TYPICAL ELECTRICAL CHARACTERISTICS

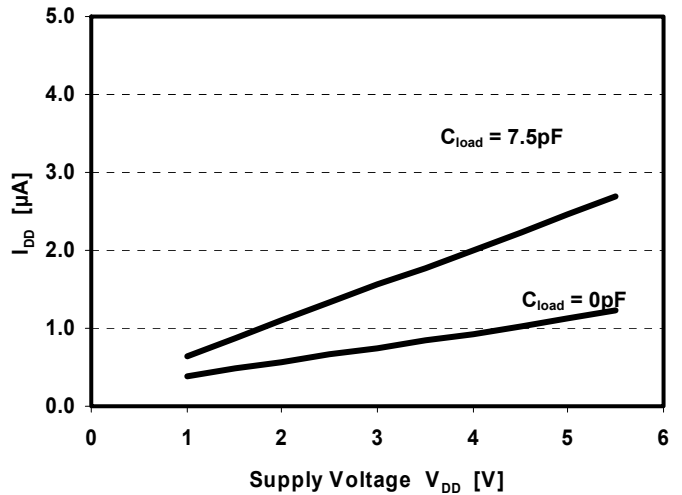
IDD Power Consumption

in "Timekeeping" or Standby-Mode.
 Conditions:
 CLKOUT Disabled



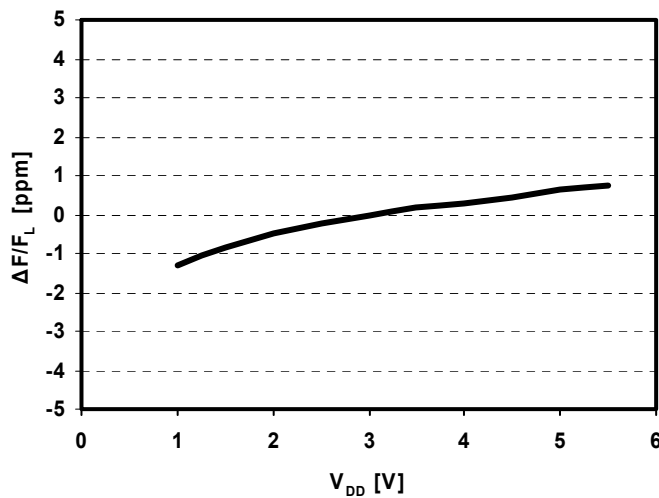
IDD Power Consumption

in "Timekeeping" or Standby-Mode.
 Conditions:
 CLKOUT Enabled
 CLKOUT-Frequency 32.768kHz



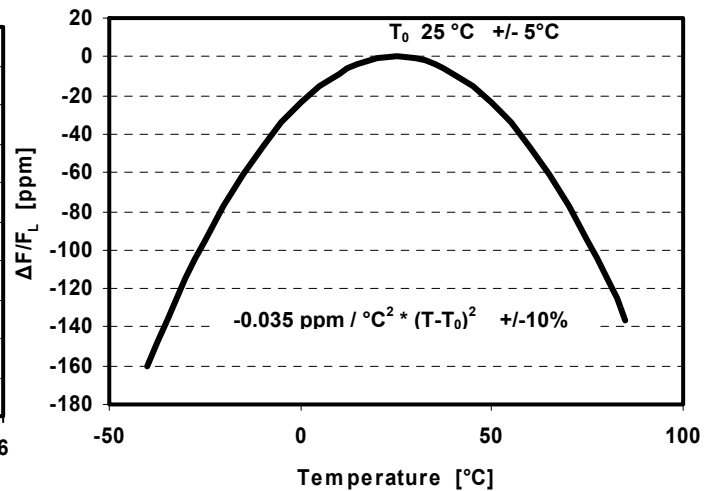
Frequency vs VDD Voltage Drift

in "Timekeeping" or Standby-Mode.
 Conditions:
 CLKOUT Enabled
 CLKOUT-Frequency 32.768kHz
 T_{ambient} 25°C



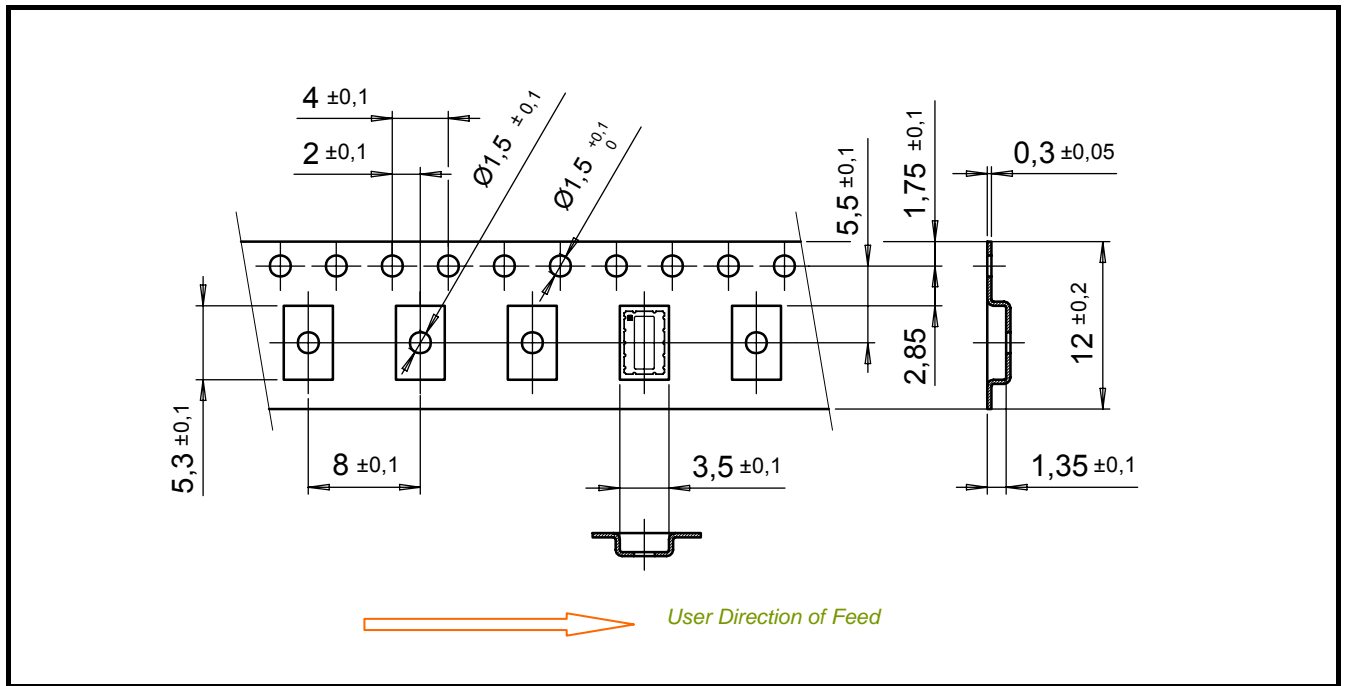
Frequency vs Temperature Drift

in "Timekeeping" or Standby-Mode.
 Conditions:
 CLKOUT Enabled
 CLKOUT-Frequency 32.768kHz
 T_{ambient} -40 to +85°C



11.0 PACKING INFO CARRIER TAPE

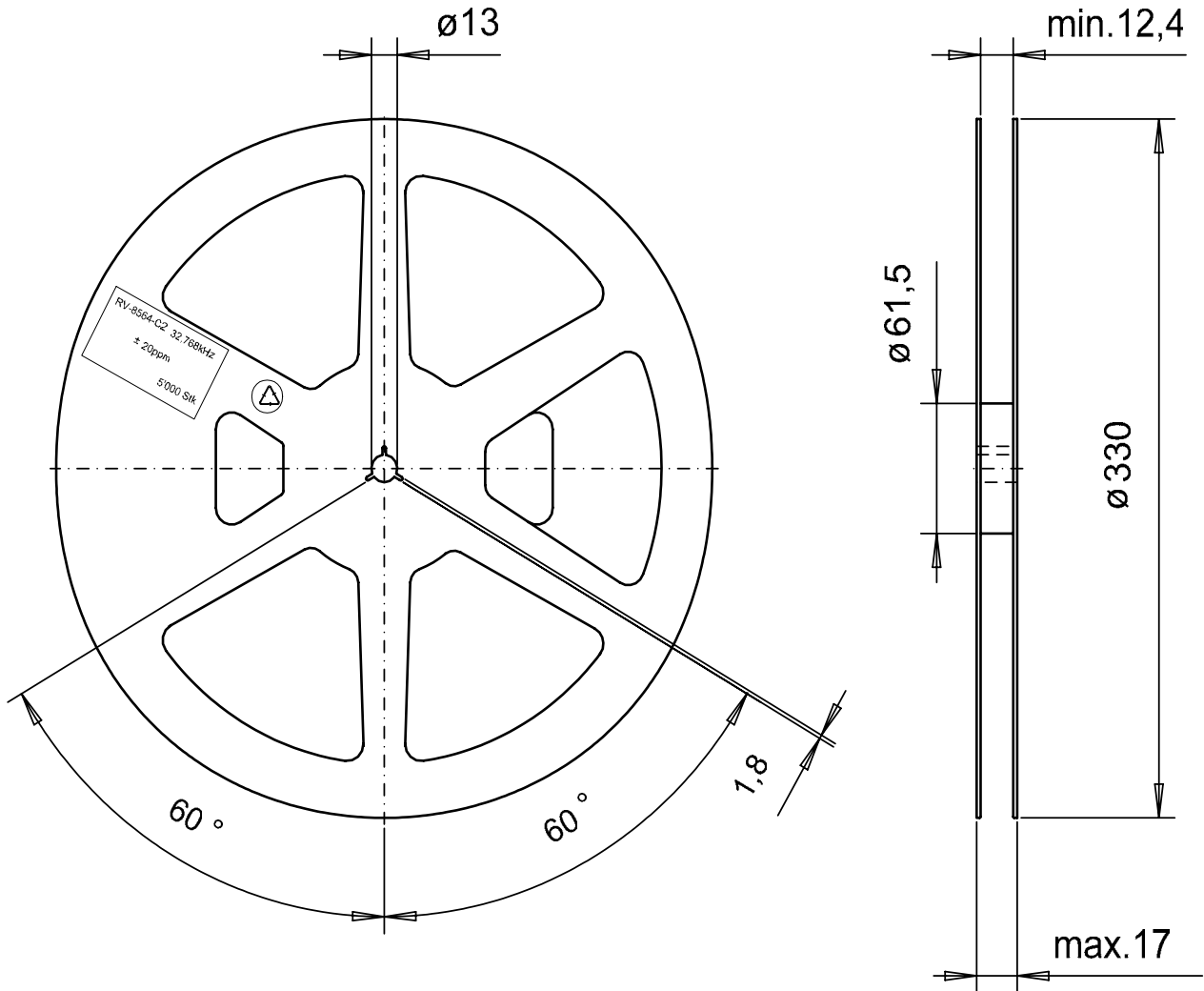
12 mm Carrier-Tape: Material: Polystyrene / Butadine or Polystyrol black, conductive
Cover Tape: Base Material: Polyester, conductive 0.061 mm
 Adhesive Material: Pressure-sensitive Synthetic Polymer



Tape Leader and Trailer: 300 mm minimum All dimensions are in mm

REELS:	DIAMETER	MATERIAL.	RTC's per REEL.
	7"	Plastic, Polystyrene	1000
	10"	Plastic, Polystyrene	2500
	13"	Plastic, Polystyrol	5000

11.1 REEL 13 INCH FOR 12 mm TAPE



Reel:

<i>Diameter</i>	<i>Material</i>
13"	Plastic, Polystyrol

12.0 DOCUMENT REVISION HISTORY

Date	Revision #	Revision Details
February 2005	1.1	First release

Information furnished is believed to be accurate and reliable. However, Micro Crystal assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. In accordance with our policy of continuous development and improvement, Micro Crystal reserves the right to modify specifications mentioned in this publication without prior notice. This product is not authorized for use as critical component in life support devices or systems.